

# ESD-induced Latch-up Testing on MK1, MK2 and MK4 ESD and Latch-up Test Systems

## Key Words

Transient Latch-up testing, ESD-induced latch-up, JEDEC78 test method

## Goal

This application note focuses on one form of Transient Latch-up testing, ESD-induced latch-up, and how it is implemented on the Thermo Scientific™ MK1, MK2 and MK4 ESD and Latch-up Test Systems.



## Latch-up – What Is It?

Latch-up is a state in which a low-impedance path (SCR) is developed between the power rails of a CMOS device, resulting in excessive power supply current consumption and is caused by an electrical overstress. The overstress can be caused by a number of different events during the operation of a device:

- **A voltage or current overstress on a signal pin or an overvoltage on the power rail.**

The JEDEC78 test method, which uses a square wave pulse as stimulus is the most widely used test method for the quasi-static latch-up test.

- **Transients, such as ESD have also been shown to cause latch-up failures.**

Although there are no industry standard test methods for ESD-induced latch-up, some internal company test methods reference the use of a low voltage Machine Model (MM) event delivered to either a signal pin or superimposed onto the power rail to trigger latch-up.

## Latch-up Testing

Latch-up testing requires that the device be powered and in a stable state prior to the latch-up stimulus being applied. As excessive supply current draw is the determination of a Latch-up failure, pre- and post-supply,  $I_{DD}$  measurements are taken on each supply rail on the device. The JEDEC78 standard's failure definition is a post-stress current increase greater than  $1.4 \times I_{nom}$  (pre-stress) supply measurement. Note: The complete JEDEC failure definition is, "If absolute  $I_{nom}$  is  $< 25$  mA, then absolute  $I_{nom} + 10$  mA is used Or If absolute  $I_{nom}$  is  $> 25$  mA, then  $> 1.4X$  absolute  $I_{nom}$  is used."

The following test sequence illustrates how the test would be performed on a signal pin.

For stressing of a supply rail, the MM event would replace the "V bias test" portion of the V bias rail shown in the drawing. It's important to note, that due to the relay matrix architecture of the MK systems, stressing of a power rail can only be archived when a device has more than one pin on its power bus. This is due to the fact that a pin cannot be connected to the bias supply and also connected to stress at the same time. If the device has more than one pin, one pin can be tied to the bias supply, while the other would be stressed. Single supply pin devices can be stressed; however, special test fixture boards would be required.

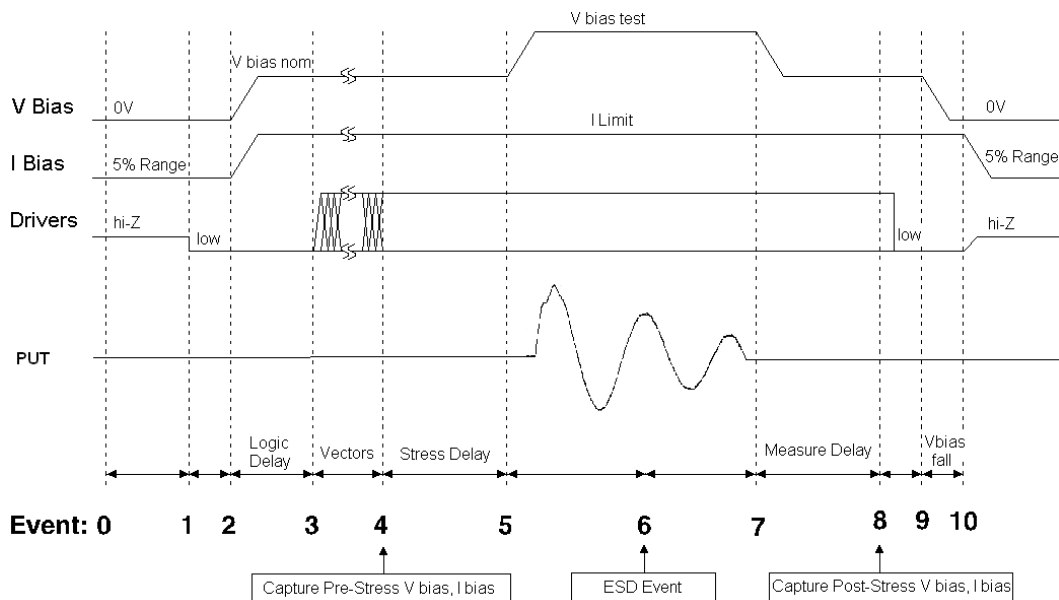


Figure 1. ESD Induced Latch-up Test Sequence (Note: The MK1 does not offer digital pin drivers)

### Implementation within the Scimitar application

With the latest release of the Scimitar application, which is used on all of our MK series of testers, the operator will

have the ability to perform ESD-induced latch-up testing using either a low voltage MM (30 to 200V) or low voltage HBM (30 to 800V) stress.

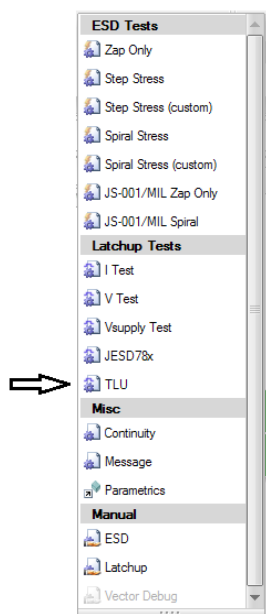


Figure 2. Test type selection (Note: The MK1 does not offer digital pin drivers)

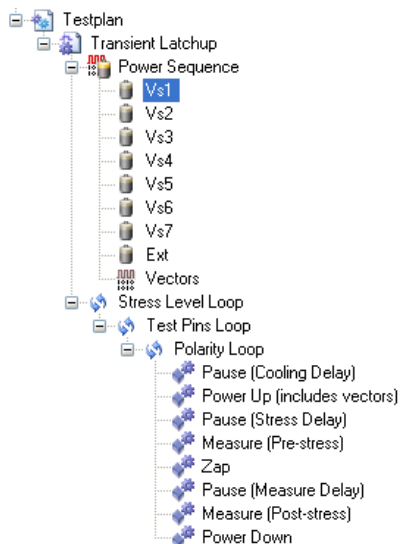


Figure 3. Test flow diagram



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